Solution : DTS 1 - 3

1.(A) Depletion layer contains only Immobile negative and positive ions.

2.(A) At room temperature, some covalent bonds break. The valence band is partly empty and conduction band is partly filled. Hence pure semiconductor behaves slightly as a conductor.

3.(D) Zener diode is used as a voltage regulator.

4.(A) Aluminium is a trivalent element.
P-type semiconductor is produced when silicon (tetravalent element) is doped with aluminum.

5.(B) Zener breakdown occurs in a semiconductor diode when reverse bias exceeds certain value.

6.(D)

7.(D) Diode design does not play any part in determining barrier potential of a P-N junction diode.

8.(C) In forward bias arrangement of P-N junction diode, depletion layer and resistance both decrease.

9.(A) At room temperature covalent bonds break in some cases and some electrons travel to conduction band with the available thermal energy. The valence band is partially empty and conduction band is partially filled as a consequence.

10.(B) The output of OR gate is one if either or both inputs are one.

11.(B) Latice constant for (f. c. c.)

$$C = r_0 \times \sqrt{2} = 2.54 \times 1.414 = 3.59 \text{ Å}$$

12.(C) P-type semiconductor is formed when germanium crystal is doped with trivalent impurities i.e. having three valuence electrons.

13.(A) The terms liquid crystal describe an intermediate state between a solid and a liquid.

14.(A) Energy gap of a semiconductor is the order of 1eV.

15.(A) Since phosphorous is pentavalent, hence its doping in Ge-crystal produces n-type semiconductor.

16.(A) Here, the P-N junction is reverse bised.
$\therefore$ Current flowing through the diode is zero.

17.(B) In reverse biased, the depletion region of P-N diode is increased.

18.(D) Current gain, $\beta = \Delta I_C / \Delta I_B = \dfrac{(10-5)mA}{(150-100)\mu A} = \dfrac{5\times10^{-1}}{50\times10^{-6}} = 100$

19.(D) We know that in a forward biased *p-n* junction diode the repulsion of holes and electrons takes place, which decreases width of potential barrier by striking the combination of holes and electrons. We also know that the options (a) and (b) show the potential barrier in reverse bias, whereas the options (c) and (d) show the potential barrier in forward bias. Moreover, the width of depletion layer in option (d) is less than shown in option (c). Thus, the potential barrier in the depletion region will be of the form as shown in option (D).

20.(B) This is an example of operational amplifier. In this voltage gain.

$$A = \frac{V_0}{V_i} = \frac{R_f}{R_i} = \frac{100k\Omega}{1k\Omega} = 100$$

21.(C) When the positive terminal of battery is connected to the p-side and negative terminal to the n-side, then diode is said to be forward biased while when negative terminal of battery is connected to p-side and positive terminal to n-side, then diode is said to be reverse biased.

22.(B) The truth table corresponding to waveform is given by :

A	B	**C**
1	1	1
0	1	0
1	0	0
0	0	0

The given logic circuit gate is AND gate.

23.(B) Reverse resistance $= \frac{\Delta V}{\Delta I} = \frac{1}{0.5 \times 10^{-6}} = 2 \times 10^{6} \Omega$

24.(D) The given truth table is for NAND gate

25.(B) In common emitter mode $\beta = \frac{I_C}{I_B}$

$I_C = \beta I_B = 80 \times 250\ \mu A$

26.(B) It is forward biased

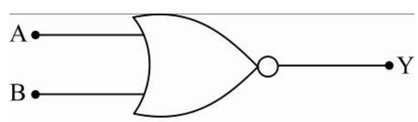
$I = \frac{\Delta V}{R} = \frac{3.2 - 3}{100 \times 10^3} = 0.2 \times 10^{-5} A$

$I = 2 \times 10^{-6} A$.

27.(B) The truth table and symbol of NOR gate is given below.

Truth table NOR gate

Input		Output
A	B	$Y = \overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0



Symbol of NOR gate

From the truth table, we can see output is high when both inputs are low

28.(A) Input resistance $R_1 = 4\Omega$

Resistance gain $= \frac{R_L}{R_i} = \frac{24\Omega}{4\Omega} = 6$

Current gain $\beta = 0.6$

Voltage gain = Current gain × Resistance gain = 0.6 × 6 = 3.6

29.(D) Given : Collector current $I_C = 9mA$

$\frac{90}{100} I_e = I_c$ [where I_e is the emitter current]

or $I_e = \frac{100}{90} \times 9\ mA = 10mA$

30.(B) Current gain $\beta = \frac{I_c}{I_b} = \frac{(120\ mA)}{(2mA)} = 60$

Power gain = Resistance gain × β^2 = (3) × $(60)^2$ = 10800

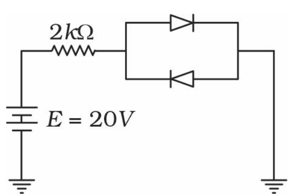
31.(C) $Y' = \overline{A + B}$ $Y = \overline{\overline{A + B}} = A + B$.

Truth table of the given circuit is given by :

A	B	Y′	Y
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

32.(D) P – type semiconductor.

33.(C)



Total resistance in the circuit $= 2k\Omega$

$$E = 20V$$

$\therefore$ The current $= \dfrac{20V}{2000\,\Omega} = 10mA$

34.(C) From the graph part CD has negative slope, thus it has negative dynamic resistance.

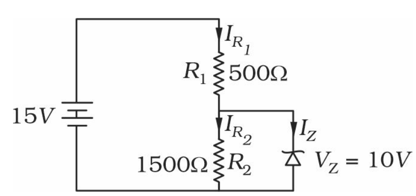
35.(D) The voltage drop across R_2 is

$$V_{R_2} = V_z = 10V$$

The current through R_2 is

$$I_{R_2} = \frac{V_{R_2}}{R_2} = \frac{10V}{1500\Omega} = 0.667 \times 10^{-2} A$$

$= 6.67 \times 10^{-3} A = 6.67\,mA$



The voltage drop across R_1 is

$$V_{R_1} = 15V - V_{R_2} = 15V - 10V = 5V$$

The current through R_1 is

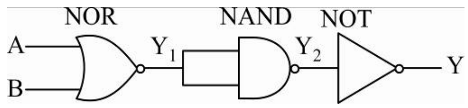
$$I_{R_1} = \frac{V_{R_1}}{R_1} = \frac{5V}{500\Omega} = 10^{-2} A = 10 \times 10^{-3} A = 10mA$$

The current through the Zener diode is

$I_Z = I_{R_1} - I_{R_2}$

$= (10 - 6.67)mA = 3.33\,mA$

36.(A)



NOR					NAND	NOT
A	B	Y_1	Y_1 A	Y_1 B	Y_2	Y
0	0	1	1	1	0	1
0	1	0	0	0	1	0
1	0	0	0	0	1	0
1	1	0	0	0	1	0

Same as NOR Gate

NOR Gate		
0	0	1
0	1	0
1	0	0
1	1	0

37.(D) Band gap = 2eV.

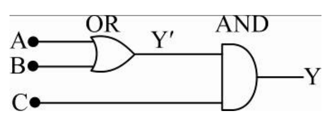
Wavelength off radiation corresponding to this energy, ; $\lambda = \frac{hc}{E} = \frac{12400\ eV\ \text{Å}}{2eV} = 6200\ \text{Å}$

The frequency of this radiation $= \frac{c}{\lambda} = \frac{3\times 10^8 m/s}{6200 \times 10^{-10} m}$ $\Rightarrow$ $\upsilon = 5 \times 10^{14} Hz$

38.(A)

A	B	Y'	C	Y
1	0	1	1	1

$\therefore$ A, B, C is 1, 0 1 to get $y = 1$.



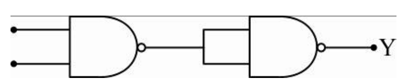
39.(B) Given $\beta = 100$

$$\beta \Delta I_B = \Delta I_C = \left(\frac{0.01V}{1000\,\Omega}\right) \times 100 = \frac{3}{R} \qquad \therefore \qquad R = 3K\Omega$$

40.(D) D_2 does not conduct as it is reverse biased. $\therefore$ Current in 10Ω is $\frac{2V}{25\Omega} = 80mA$

41.(A) $\overline{A \cdot B} \rightarrow \overline{\overline{A \cdot B}} = A \cdot B$ (AND gate)

			Y
$A = 0,$	$B = 0,$	$\overline{Y} = 1$	0
$A = 0,$	$B = 1,$	$\overline{Y} = 1$	0
$A = 1,$	$B = 0,$	$\overline{Y} = 1$	0
$A = 1,$	$B = 1,$	$\overline{Y} = 0$	1



42.(B) The break down field of the Zener diode = 10^6 V/m.

The width of the depletion region = 2.5×10^{-6} m.

$\therefore$ $V_{\text{breakdown}} = E \times d = 10^6 \times 2.5 \times 10^{-6}$ $\Rightarrow$ $V_{\text{breakdown}} = 2.5$ V

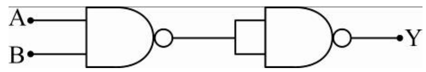
43.(C)

44.(A) The number of electrons or holes or intrinsic charge carrier concentration at temperature TK is given by

$ni = AT^{3/2}\ e^{-E_{g/2kT}}$

Where A is a constant, Eg is the forbidden energy gap at 0 K in eV, k is the Boltzmann constant.

45.(B) 2NAND are required to form an AND gate. The given circuit diagram is shown below.



Solution : JEE Main (Archive)

1.(B) Variation of the number charge carriers with temperature. FACT

2.(C) As we go from p to n side in a reverse biased p-n junction potential increases

3.(A) When npn transistor is used, majority charge carrier electrons of n type emitter move from emitter to base and then base to collector.

4.(D) In CE configuration, $A_i = \dfrac{-h_{fe}}{1+h_{0e}R_L} = \dfrac{-50}{1+25\times10^{-6}\times1\times10^3} = -48.78$

5.(C) Copper is metallic conductor and germanium is semiconductor therefore as temperature decreases resistance of good conductor decreases while for semiconductor it increases. **6.(B)** FACT

7.(C) P is connected to +ive and N side to – ive $\therefore$ Both reduces **8.(C)** FACT

9.(C) $E_g = \dfrac{hc}{\lambda} = 0.5\ eV$

10.(C) frequency = 2 (frequency of input signal).

11.(C) No phase difference between input and output signal.

12.(C) Covalent binding . Property refers to semiconductor which has covalent bonds.

13.(D) $\dfrac{n_e}{n_h} = \dfrac{7}{5}$; $\dfrac{I_e}{I_h} = \dfrac{7}{4}$; $\dfrac{(V_d)_e}{(V_d)_h} \Rightarrow \dfrac{I_e}{I_h}\times\dfrac{n_h}{n_e} = \dfrac{5}{4}$

14.(B) $I_b = I_e - I_c$; $\beta = \dfrac{I_c}{I_b} = 49$

15.(D) Lattice constant refers to physical dimension of unit cells in a crystal lattice. If it is decreased E_C & E_V decreases but E_g increases.

16.(A) Only in (A) on going from p to n side potential increase.

17.(C) D_1 is reverse biased therefore it will act like an open circuit.

$i = \dfrac{12}{6} = 2.00A$

18.(D) For $V_i < 0$, the diode is reverse biased and hence offer infinite resistance so $V_0 = 0$

For $V_i > 0$, diode is forward biased, so, $V_0 = V_i$

19.(D) C is insulator Si and Ge are semiconductors. **20.(A)**

21.(D) Truth table show its OR gate

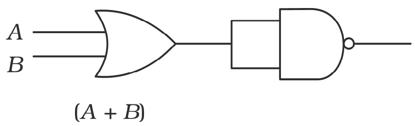
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

22.(A) Truth table for given combination is

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

This comes out to be truth table of OR gate

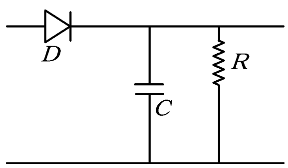
23.(D)



24.(A) They are two individual NOT gates and when they combine they form a NAND gate.

25.(D) For LED, in forward bias, intensity increases with voltage.

26.(A) $\tau = RC = 2.5 \times 10^{-5}$ and Highest Frequency



$= \dfrac{1}{2\pi m_a RC} = 10.62\ kHz$

27.(A) D_1 & D_2 conducts as they are forward biased D_3 doesn't conduct.

$\therefore \quad i = \dfrac{6}{R_3 + R_1 + R_{D_1}} = \dfrac{6}{50 + 50 + 20} \quad ; \quad \dfrac{6}{120} = 50mA$

28.(A) Verify by using truth table. **29.(C)** Only in C potential difference across diode > 0.

30.(C) $I_L = V_z / R_L = 5mA \; I = 60 - V_z / 4000 = 12.5mA \; \therefore \quad I_z = 7.5\,mA$

31.(B) Self Explanatory

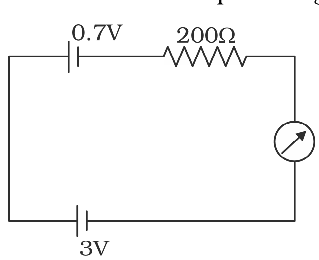
32.(AC) $\beta = \dfrac{\alpha}{1-\alpha}$, is not satisfied by option (A, C)

33.(B) From truth Table, it is OR gate. **34.(D)** FACTUAL

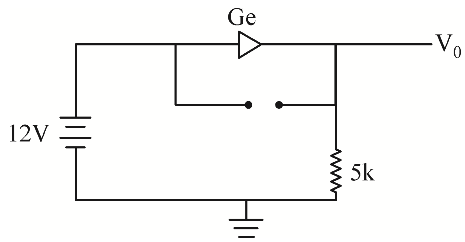
35.(D) Spectral Range of Visible light is from $0.4\,\mu m$ to $0.7\ \mu m$ i.e., 3eV to 1.8 eV.

36.(A) In common emitter amplifier circuit the output voltage is out of phase w.r.t. input voltage.

37.(D) $I = \dfrac{3-0.7}{200} A = 11.5\ mA$



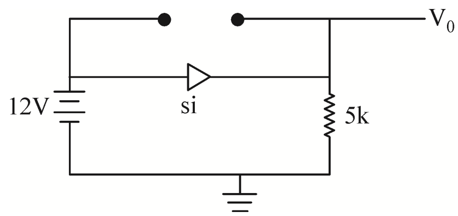
38.(C) Initially



Silicon diode will behave like open circuit

So $V_0 = 12 - 0.3 = 11.7V$

Finally Ge is reverse biased and it will not conduct as per assumption so



$V_0 = 12 - 0.7 = 11.3V$

Change $= 0.4V$

39.(D) If contribution of holes is neglected, then

$$I = neAv_e = neA\mu_e E \quad \Rightarrow \quad \frac{VA}{\rho\ell} = neA\mu_e E$$

$$\Rightarrow \quad \rho = \frac{1}{ne\mu_e} = \frac{1}{10^{19} \times 1.6 \times 10^{-19} \times 1.6} = \frac{100}{(16)^2} = 0.39\Omega - m \approx \boxed{0.4\Omega m} \text{ i.e. option (D)}$$

40.(A) Voltage drop across $10k\Omega = 50V$

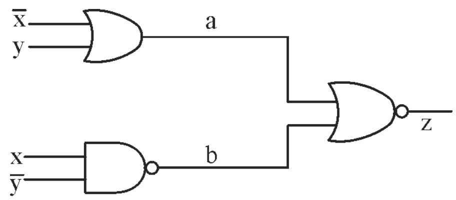
$$i_{10k\Omega} = \frac{50}{10 \times 10^3} A = 5mA$$

Voltage drop across $5k\Omega = 70V$

$$i_{5k\Omega} = \frac{70}{5 \times 10^3} = 14mA$$

Hence, current through zener diode $= (14 - 5)mA = 9mA$

41.(A)



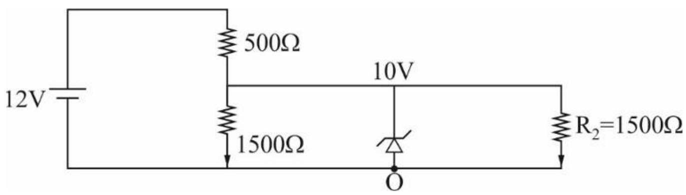
x	y	$\bar{x}$	$\bar{y}$	a	b	z
0	0	1	1	1	1	0
0	1	1	0	1	1	0
1	0	0	1	0	0	1
1	1	0	0	1	1	0

$\therefore$ *For* $z = 1$, $x = 1$ and $y = 0$

42.(D) As the given diodes are ideal diodes. Current in D_2 should be zero.

$\therefore \quad i = \dfrac{6}{50+150+100}$ or $i = 0.020\ A.$

43.(C) Voltage across $R_2 = 10V$.



So, $i(R_2) = \dfrac{10}{1500} = \dfrac{2}{3} \times 10^{-2} A$

So, current through $500\,\Omega = \left(\dfrac{4}{3} \times 10^{-2} + i_z\right)$

So, voltage across $500\ \Omega = \left(\dfrac{20}{3} + 500 i_z\right)$

So, $\quad 12 - 10 = \dfrac{20}{3} + 50 i_z$

This gives a negative value of i_z.

So, $\quad i_z = 0$.

44.(C) $V_{CC} - \beta I_B R_C = 0$

$I_B = \dfrac{5}{200 \times 10^3} = 2.5 \times 10^{-5} A = 25\mu A$; $\quad V_{BB} - I_B R_B - 1 = 0$

$V_{BB} = 25 \times 10^{-6} \times 100 \times 10^3 + 1 = 3.5V$

45.(D) $Y=\overline{\overline{A.\overline{AB}}.\overline{\left(A\overline{B}+B\right)}}$

$Y=\overline{\overline{A.\overline{AB}}}+\overline{\overline{AB}+B}$

$=A.\overline{AB}+AB.\overline{B}$

$=A.\left(\overline{A}+\overline{B}\right)+\left(AB\right).\overline{B}$

$=A\overline{B}+0$

46.(D) Potential drop across $800\,\Omega$ resistor = 5.6 V

$\Rightarrow$ Current through $800\,\Omega$ resistor $=\dfrac{5.6}{800}A$

$\Rightarrow$ Current through $200\,\Omega$ resistor $=\dfrac{9-5.6}{200}=\dfrac{3.4}{200}$

$\Rightarrow$ Current through Zener diode $=\dfrac{3.4}{200}-\dfrac{5.6}{800}=\dfrac{8}{800}\Rightarrow 10mA$

47.(A) $\Delta I_C=\dfrac{V_{CC}}{R_C}$

$\beta=\dfrac{\Delta I_C}{\Delta I_B}$

$\Delta I_B=\dfrac{\Delta I_C}{\beta}=\dfrac{V_{CC}}{R_C.\beta}$

Putting the values we get

$\Delta I_B=40\mu A$

48.(C) input resistance = $r=\dfrac{10mV}{15\times10^{-6}}=0.67\ K\Omega$

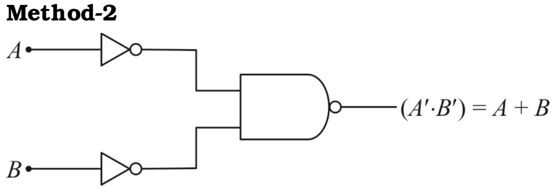
Voltage gain = $+\beta\dfrac{Rc}{r}=+\dfrac{3mA}{15\mu A}\times\dfrac{1K\Omega}{0.67K\Omega}=+300\ Volt$

49.(D) Truth table can be formed as

A	*B*	*Equivalent*
0	0	0
0	1	1
1	0	1
1	1	1

Hence the equivalent is "OR" gate

Method-2



OR (GATE)

50.(B) $V_L = 6V \qquad i_L = \dfrac{6}{4\times 10^3} = 1.5\times 10^{-3}A$

$V_B = 8V \qquad i_{Ri} = \dfrac{16-6}{1\times 10^3} = 10\times 10^{-3}A$

$i_{zener} = 2\times 10^{-3} - 1.5\times 10^{-3} = 8.5\times 10^{-3}A$

$V_B = 16V \qquad iR_i = \dfrac{16-6}{1\times 10^3} = 10\times 10^{-3}$

$i_{zener} = 10\times 10^{-3} - 1.5\times 10^{-3} = 8.5\times 10^{-3}$

51.(C) $10\log_{10}\left(\dfrac{P_{out}}{P_{in}}\right) = 60 \Rightarrow \dfrac{P_{out}}{P_{in}} = 10^6.$

$P_{out} = \Delta V_{out}\cdot \Delta I_C$

$P_{in} = \Delta V_{in}\cdot \Delta I_B$

$\because \quad V_{out} = I_C\cdot R_{out} \Rightarrow \Delta V_{out} = R_{out}\cdot \Delta I_C \quad \because \quad V_{in} = I_B\cdot R_{in} \Rightarrow \Delta V_{in} = R_{in}\cdot \Delta I_B$

$\dfrac{R_{out}}{R_{in}}\cdot \beta^2 = 10^6$

$\beta = 100$

52.(D) $V_z = 6V$

$V = 1R_s + V_z \qquad \{V_{mass} = 16volt\}$

$16 = 1R_s + 6$

$iR_s = 10 \qquad i = \dfrac{10}{2\times 10^3} = 5mA$

This current will be divided

$V_z = I_L R_L$

$\dfrac{6}{4} = I_L \qquad \Rightarrow \qquad i_L = 1.5mA$

So current through Zener = 3.5 mA

53.(C) $A = 0, B = 0, Y = 1$

$A = 0, B = 1, Y = 1$

$A = 1, B = 0, Y = 0$

$A = 1, B = 1, Y = 0$

54.(B) $R_i = 100\Omega$

$R_{output} = 100\times 10^3\Omega$

Voltage gain = $\dfrac{\text{change in output voltage}}{\text{change in input voltage}}$

Voltage gain $= \dfrac{\Delta V_0}{\Delta V_i}$

$= \dfrac{\Delta I_C \times R_0}{\Delta I_b \times R_i}$

$A_v = 5 \times 10^4$

Power gain $= \dfrac{\text{change in output power}}{\text{change in input power}} = \dfrac{\Delta V_0 \cdot \Delta I_C}{\Delta V_i \cdot \Delta I_b} = \dfrac{\Delta I_C \cdot R_0 \cdot \Delta I_C}{\Delta I_b \cdot R_i \times \Delta I_b} = \left(\dfrac{\Delta I_C}{\Delta b}\right)^2 \times \dfrac{R_0}{R_i}$

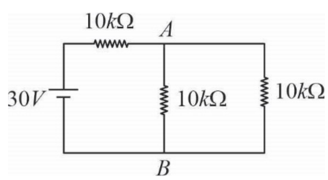
$= \left(\dfrac{5 \times 10^{-3}}{100 \times 10^{-6}}\right)^2 \times \dfrac{100 \times 10^3}{100} = \dfrac{25 \times 10^{-6}}{10^{-8}} \times 10^3$

Power gain $= 25 \times 10^5 = 2.5 \times 10^6$

55.(B) A logic gate is reversible if we can recover input data from the output.

56.(C) Diode is in forward Bias

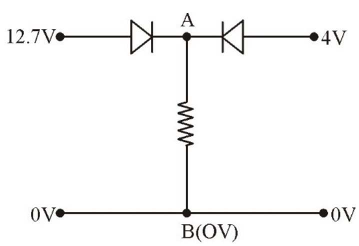
$V_{AB} = \left(\dfrac{5}{5+10}\right) \times 30 = 10V$



57.(B) First part of figure shown OR gate and
Second part of figure shown NOT gate
So Y_p = OR + NOT = NOR gate

$Y = \overline{A+B} = \bar{A} \cdot \bar{B}$

58.(12)



Assume $V_B = 0V$

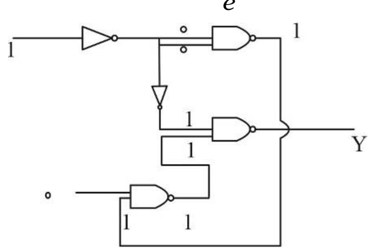
Hence right diode is reversed bias. As built in potential is $0.7V \Rightarrow V_A = 12V$

59.(A) $I = \dfrac{V}{R(net)} = \dfrac{9}{(10+5+10+5)} = \dfrac{9}{30} = 0.3A$

60.(A) $Q_A = VC$ open circuit due to reverse biased diode

$Q_B = VCe^{-t/RC} = \dfrac{VC}{e}$ due to forward biased diode

61.(C)



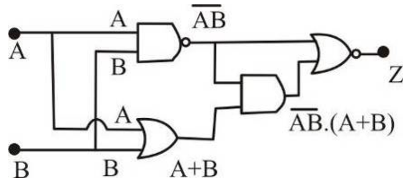
62.(40) Potential difference across resistors = 12 – 8 = 4V

$I=\frac{4}{400}=\frac{1}{100}A$

P.d across each Zener diode $=\frac{8}{2}=4V$

Power dissipated $=VI=(4)\left(\frac{1}{100}\right)=40\times10^{-3}\ W=40\ mW$

63.(A) Logic gate



$Z=\overline{\overline{AB}+\overline{AB}.(A+B)}=\overline{\overline{AB}+(\overline{A}+\overline{B}).(A+B)}$

$=\overline{\overline{AB}+(\overline{A}.A+\overline{A}.B+\overline{B}A+B\overline{B})}=\overline{\overline{AB}+(0+\overline{A}.B+\overline{B}A+0)}$

$=\overline{\overline{A}+\overline{B}+\overline{A}B+\overline{B}A}=\overline{\overline{A}(1+B)+\overline{B}(1+A)}=\overline{\overline{A}+\overline{B}}=AB$

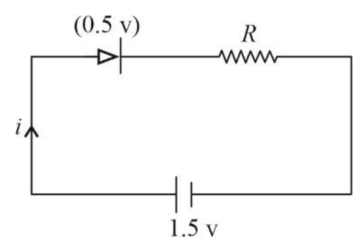
64.(B) $i=\left(\frac{1.5-0.5}{R}\right)$

$i=\left(\frac{1}{R}\right)$

$\because\qquad i\le 10\ mA$

$\Rightarrow\qquad \frac{1}{R}\le10\times10^{-3}\ \Rightarrow\ R\ge100\ \Omega$

$\Rightarrow\qquad R_{\min}=100\Omega$



65.(B) Multimeter in resistance mode, measures resistance of the component. If we connect capacitor it will show reading which increases gradually (if capacitor is uncharged initially) and finally reading will stabilize at high value.

66.(A) Band gap energy $=\frac{hc}{\lambda}$

Putting values of h,c and λ

Band gap energy $=3.1eV$

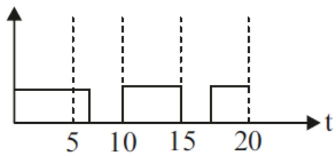
67.(C) $V_{0_{\max}}=V_{in}-V_z=10V-6V$; $\quad V_{0(\max)}=4V$

68.(B)

69.(B)

70.(None) Truth table for the given combination is

Correct output



A	B	Y
1	1	1
1	0	1
0	1	1
0	0	0

71.(150)

$\Delta I_B = (30-20)\mu A = 10\mu A,\ \Delta I_C = (4.5-3.0)mA = 1.5mA$

Therefore, $\beta_{ac} = 1.5mA / 10\mu A = 150$